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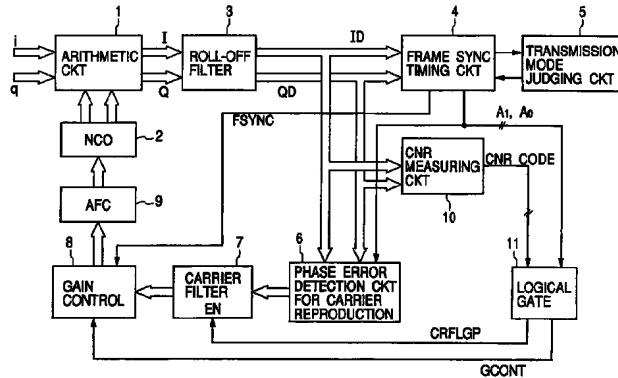
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**(54) HIERARCHICAL TRANSMISSION DIGITAL DEMODULATOR**

(57) There is proceeded hierarchical transmission digital demodulator capable of stable sync capture and stable demodulation through setting of a demodulation operation in accordance with a reception C/N value. A CNR measuring circuit 10 receives a demodulation output from an arithmetic circuit 1 and measures a reception C/N value. During a period until a sync is captured, a carrier is reproduced in accordance with the demodulation output that a modulated wave in a header section and a modulated wave of burst symbol signal.

After the sync is captured, at an intermediate C/N value the carrier is reproduced in accordance with the demodulation output of the header section, burst symbol signal and QPSK signal and in accordance with output from a logical gate circuit 11, and at high and low C/N values the carrier is reproduced by setting high a carrier reproduction loop gain of a gain control circuit 8 in accordance with a signal from the logical gate circuit 11.

**FIG. 1**

**Description****FIELD OF THE INVENTION**

[0001] The present invention relates to a hierarchical transmission digital demodulator for demodulating digital modulated waves multiplexed on a time axis by a plurality of modulation methods in which necessary C/N (ratio of carrier power to noise power) values are different.

**DESCRIPTION OF THE RELATED ART**

[0002] A hierarchical transmission method is known by which digital modulated waves multiplexed on a time axis by a plurality of modulation methods in which necessary C/N values, e.g., 8PSK modulation waves, QPSK modulation waves and BPSK modulation waves, are combined to form frames which are repetitively transmitted. With such a hierarchical transmission method, since BPSK modulation waves (including burst symbol signals) provide a wide lock-in range and are easy to capture sync, the sync capture is obtained by receiving the BPSK modulation waves (including burst symbol signals) and after the sync capture is obtained, sequentially input BPSK modulation signals, burst symbol signals (BPSK modulation signals), QPSK modulation signals and 8PSK modulation signals are demodulated (continuously demodulated) in the order of input signals.

[0003] However, if the reception C/N value is degraded during the continuous demodulation, the reception state of 8PSK modulation waves requiring a high necessary C/N value is degraded. Therefore, at the receivable limit C/N value of lower hierarchical QPSK or BPSK modulation waves, a carrier slip occurs in the section of 8PSK modulation waves and the frame sync of the system cannot be captured. The necessary C/N value is therefore substantially raised and the reception state becomes unstable.

[0004] It is an object of the present invention to provide a hierarchical transmission digital demodulator capable of stable sync capture and stable demodulation by setting a demodulation operation in accordance with the reception C/N value.

**DISCLOSURE OF THE INVENTION**

[0005] A hierarchical transmission demodulator of this invention comprises: first carrier reproducing means for reproducing a carrier in accordance with demodulation outputs that a modulated wave in a header section and a modulated wave of a burst symbol signal are demodulated; means for measuring a reception C/N value; second carrier reproducing means for reproducing the carrier in accordance with continuous demodulation outputs if the measured reception C/N value after the sync capture is equal to or larger than a

first predetermined threshold; third carrier reproducing means for reproducing the carrier in accordance with demodulation outputs for a hierarchical level except a high hierarchical level if the measured reception C/N value which is equal to or larger than a second threshold which is lower than the first threshold.

[0006] According to the hierarchical transmission demodulator of this invention, during the period until sync is captured, the carrier is reproduced by the first carrier reproducing means in accordance with demodulation outputs that a modulated wave in a header section and a modulated wave of a burst symbol signal are demodulated. Accordingly, the carrier can be reproduced reliably. A reception C/N value is measured by the C/N measuring means and if the reception C/N value after the sync capture is equal to or larger than the first predetermined threshold after the sync capture, the carrier is reproduced by the second carrier reproducing means in accordance with the continuous demodulation output. It is therefore possible to prevent jitters, etc. to be caused by inability of following a frequency change while the carrier is not reproduced. If the measured reception C/N value after the sync capture is equal to or larger than the second threshold which is lower than the first threshold, the carrier is reproduced by the third carrier reproducing means in accordance with demodulation outputs for a hierarchical level except a high hierarchical level.

[0007] The hierarchical transmission digital demodulator of this invention further comprises reproduction loop characteristic switching means for switching a carrier reproduction to a different carrier reproduction characteristic during carrier reproduction by the first carrier reproducing means and during carrier reproduction by the carrier reproducing means different from the first carrier reproducing means.

[0008] According to the hierarchical transmission digital demodulator of this invention, the reproduction loop characteristic is switched between different carrier reproduction characteristics during carrier reproduction by the first carrier reproducing means and during carrier reproduction by the carrier reproducing means different from the first carrier reproducing means.

**BRIEF DESCRIPTION OF THE DRAWINGS****[0009]**

Fig. 1 is a block diagram showing the structure of a hierarchical transmission digital demodulator according to an embodiment of the invention.

Figs. 2(a) - 2(d) shows the structure of a frame used by a hierarchical transmission method and waveforms of signals AI and AO, according to the embodiment of the invention.

Fig. 3 is a block diagram showing the structures of an arithmetic circuit, a numerical control oscillator and an AFC circuit, respectively of the hierarchical

transmission digital demodulator according to the embodiment of the invention.

Fig. 4 is a diagram showing the relation between a transmission mode and a hierarchical combination used by a transmission mode judging circuit of the hierarchical transmission digital demodulator according to the embodiment of the invention.

Fig. 5 is a diagram illustrating a demodulation ROM table of the hierarchical transmission digital demodulator according to the embodiment of the invention.

Fig. 6 is a diagram showing the relation between a loop gain and a logical value of a gain control circuit of the hierarchical transmission digital demodulator according to the embodiment of the invention.

Figs. 7(a) and 7(b) are a diagram illustrating a phase error table (for a BPSK signal) of the hierarchical transmission digital demodulator according to the embodiment of the invention.

Figs. 8(a) and 8(b) are a diagram illustrating a phase error table (for a QPSK signal) of the hierarchical transmission digital demodulator according to the embodiment of the invention.

Figs. 9(a) and 9(b) are a diagram illustrating a phase error table (for an 8PSK signal) of the hierarchical transmission digital demodulator according to the embodiment of the invention.

Fig. 10 is a characteristic diagram illustrating CNR measurements by the hierarchical transmission digital demodulator according to the embodiment of the invention.

Fig. 11 is a diagram showing the relation between a CNR code output from a CNR measuring circuit and a C/N value of the hierarchical transmission digital demodulator according to the embodiment of the invention.

Fig. 12 is a block diagram showing a logical gate circuit of the hierarchical transmission digital demodulator according to the embodiment of the invention.

Fig. 13 is a flow chart illustrating the operation of the hierarchical transmission digital demodulator according to the embodiment of the invention.

#### EMBODIMENTS OF THE INVENTION

**[0010]** An embodiment of a hierarchical transmission digital demodulator of this invention will be described.

**[0011]** Fig. 1 is a block diagram showing the structure of a hierarchical transmission digital demodulator according to an embodiment of the invention.

**[0012]** Prior to describing the hierarchical transmission digital demodulator according to the embodiment of the invention, the structure of a frame used by the hierarchical transmission system will be described. Fig. 2(a) is a diagram showing an example of the frame structure used by the hierarchical transmission system.

One frame is constituted of one header of 192 symbols and a plurality of pairs of 203 symbols and 4 symbols, totalling in 39936 symbols.

**[0013]** More specifically, one frame is constituted of: 5 a frame sync pattern (BPSK) of 32 symbols; a transmission and multiplexing configuration control pattern (TMCC) (BPSK) of 128 symbols for transmission and multiplexing configuration identification; a super-frame identification information pattern of 32 symbols; a main signal (TC8PSK) of 203 symbols and a burst symbol signal (BPSK) of 4 symbols (indicated by BS in Fig. 2(a)); a main signal (TC8PSK) of 203 symbols and a burst symbol signal of 4 symbols; , , ; a main signal (QPSK) of 203 symbols and a burst symbol signal of 4 symbols; and a main signal (QPSK) of 203 symbols and a burst symbol signal of 4 symbols, respectively arranged in this order. 8 frames are called a super-frame and the super-frame identification information pattern is used for identifying the super-frame. 192 symbols from the frame sync pattern to the end of the super-frame identification information pattern is also called the header.

**[0014]** Next, the hierarchical transmission digital demodulator according to the embodiment of the invention will be described. The hierarchical transmission digital demodulator has an arithmetic circuit 1, a numerical control oscillator 2, a roll-off filer 3 composed of a digital filter having the raised cosine characteristics, a frame sync timing circuit 4, a transmission mode judging circuit 5, a carrier reproduction phase error detection circuit 6, a carrier filer 7 composed of a low-pass digital filter, a gain control circuit 8, an automatic frequency control (AFC) circuit 9, a CNR measuring circuit 10 and a logical gate circuit 11.

**[0015]** As shown in Fig. 3, the AFC circuit 9 has a cumulative adder 91 and a latch circuit 92 which latches an output of the cumulative adder 91 and outputs it to the cumulative adder 91. As shown in Fig. 3, the numerical control oscillator 2 has a sine table 23 for receiving a latch output from the latch circuit 92 to output sine data 23a and 23b of opposite polarities and a cosine table 24 for receiving the latch output from the latch circuit 92 to output cosine data 24a and 24b. In accordance with the output from the latch circuit 92, the numerical control oscillator 2 outputs the sine data 23a and 23b and cosine data 24a and 24b of opposite polarities, to output sine and cosine signals of opposite polarities which substantially form a reproduction carrier in cooperation with the AFC circuit 9.

**[0016]** The arithmetic circuit has, as shown in Fig. 3,: a multiplier 1a for multiplying a quasi-sync detected I axis baseband signal i by the sine data 23a; a multiplier 1b for multiplying the baseband signal i by the cosine data 24a; a multiplier 1d for multiplying a quasi-sync detected Q axis baseband signal q by the opposite polarity sine data 23b; a multiplier 1e for multiplying the baseband signal q by the cosine data 24b; an adder 1c for adding outputs of the multipliers 1b and 1d to output

the addition result as a baseband signal I, and an adder 1f for adding outputs of the multipliers 1a and 1e to output the addition result as a baseband signal Q. The arithmetic circuit 1 therefore tunes the frequencies of the baseband signals I and Q and outputs the frequency tuned baseband signals I and Q to the roll-off filter 3.

**[0017]** Upon reception of baseband signals ID and QD output from the roll-off filter 3, the frame sync timing circuit 4 outputs a TMCC pattern to the transmission mode judging circuit 5. In accordance with the decoded result of the TMCC pattern, the transmission mode judging circuit 5 supplies the frame sync timing circuit 4 with a 2-bit transmission mode signal shown in Fig. 4 and representing a hierarchical combination of: an 8PSK signal which is a high hierarchical signal (demodulation output that the 8PSK modulated signal is demodulated is referred to as an 8PSK signal); a QFSK signal which is a low hierarchical (demodulation output that the QPSK modulated signal is demodulated is referred to as a QPSK signal); the 8PSK signal and QPSK signal; and the 8PSK signal and BPSK signal (demodulation output that the BPSK modulated signal is demodulated is referred to as a BPSK signal).

**[0018]** As shown in Fig. 4, the transmission mode signal takes a value "00" for the 8PSK signal, a value "01" for the QPSK signal, a value "10" for the 8PSK signal and QPSK signal, and a value "11" for the 8PSK signal and BPSK signal.

**[0019]** The frame sync timing circuit 4 receives the baseband signals ID and QD to detect a sync pattern and output a frame sync signal FSYNC, and also receives the transmission mode signal to output a signal AI shown in Fig. 2(b) which takes a high level during the header section and burst symbol signal section, and a signal AO shown in Fig. 2(c) which takes a high level during the QPSK signal section.

**[0020]** The carrier reproduction phase error detection circuit 6 receives the baseband signals ID and QD and signals AI and AO to detect a phase error and output a phase error voltage corresponding to the detected phase error. More specifically, the carrier reproduction phase error detection circuit 6 is provided with a phase error table for the BPSK signal shown in Figs. 7(a) and (b), a phase error table for the QPSK signal shown in Figs. 8(a) and 8(b), and a phase error table for the 8PSK signal shown in Figs. 9(a) and 9(b). The carrier reproduction phase error detection circuit 6 judges the transmission mode in accordance with the signals AI and AO, selects the phase error table in accordance with the judged transmission mode, obtains the phase from the signal point arrangement of the baseband signals ID and QD, and outputs a phase error voltage corresponding to the phase.

**[0021]** For example, if it is judged that the transmission mode corresponds to the BPSK signal (signals AI and AO are "1, 0") having the standard positions of the signal points at 0 ( $2\pi$ ) radian and  $\pi$  radian, then the carrier reproduction phase error detection circuit 6 selects

the phase error table shown in Figs. 7(a) and 7(b), and outputs: a negative phase error voltage shown in Fig. 7(a) for the phase in an increase direction in the range from the phase equal to or larger than  $3\pi/2$  radian to the phase smaller than 0 ( $2\pi$ ) radian; a positive phase error voltage shown in Fig. 7(a) for the phase in a decrease direction in the range from the phase smaller than  $\pi/2$  radian to the phase larger than 0 ( $2\pi$ ) radian; a negative phase error voltage shown in Fig. 7(a) for the phase in an increase direction in the range from the phase equal to or larger than  $\pi/2$  radian to the phase smaller than  $\pi$  radian; and a positive phase error voltage shown in Fig. 7(a) for the phase in a decrease direction in the range from the phase smaller than  $3\pi/2$  radian to the phase larger than  $\pi$  radian. The phase error voltage takes the maximum value in the increase direction (+) at  $3\pi/2$  radian and the maximum value in the decrease direction (-) at  $\pi/2$  radian.

**[0022]** If it is judged that the transmission mode corresponds to the QPSK signal (signals AI and AO are "0, 1") having the standard positions of the signal points at  $\pi/4$  radian,  $3\pi/4$  radian,  $5\pi/4$  radian and  $7\pi/4$  radian, then the carrier reproduction phase error detection circuit 6 selects the phase error table shown in Figs. 8(a) and 8(b). In this case, the phase error voltage takes the + direction maximum value or - direction maximum value at the phase of 0 ( $2\pi$ ) radian,  $\pi/2$  radian,  $\pi$  radian or  $3\pi/4$  radian, the maximum value being a half of that of the BPSK signal. The description for the phase error voltage to be output when the transmission mode corresponds to the QPSK signal is omitted, since this can be easily understood from the description for the transmission mode for the BPSK signal.

**[0023]** If it is judged that the transmission mode corresponds to the 8PSK signal (signals AI and AO are "0, 0") having the standard positions of the signal points at 0 ( $2\pi$ ) radian,  $\pi/4$  radian,  $\pi/2$  radian,  $3\pi/4$  radian,  $\pi$  radian,  $5\pi/4$  radian,  $3\pi/2$  radian and  $7\pi/4$  radian, then the carrier reproduction phase error detection circuit 6 selects the phase error table shown in Figs. 9(a) and 9(b). In this case, the phase error voltage takes the + direction maximum value or - direction maximum value at the phase of  $\pi/8$  radian,  $3\pi/8$  radian,  $5\pi/8$  radian,  $7\pi/8$  radian,  $9\pi/8$  radian,  $11\pi/8$  radian,  $13\pi/8$  radian, or  $15\pi/8$  radian, the maximum value being a quarter of that of the BPSK signal. The description for the phase error voltage to be output when the transmission mode corresponds to the 8PSK signal is omitted, since this can be easily understood from the description for the transmission mode for the BPSK signal.

**[0024]** The phase error voltage output from the carrier reproduction phase error detection circuit 6 is supplied to the carrier filter 7 composed of a digital low-pass filter to smooth the phase error voltage. In this case, the filtering operation is selectively executed in accordance with a CNR code output from the logical gate circuit 11 to be described later and with a carrier filter control signal (CRFLGP) suitable for the mode identified by the

signals AI and AO.

**[0025]** An output of the carrier filter 7 is supplied to the gain control circuit 8 which controls the gain in accordance with a gain control signal (GCONT) output from the logical gate circuit 11 for each of a high C/N value and an intermediate C/N value. For example, as shown in Fig. 6, if the gain control signal (GCONT) takes a high potential, a high gain, such as a gain of amplifying the output of the carrier filter two times, is set, whereas if the gain control signal (GCONT) takes a low potential, a low gain, such as a unity gain of outputting the output of the carrier filter 7 as it is, is set. An output of the gain control circuit 8 is supplied to the AFC circuit. Namely, the output is supplied to the cumulative adder 91 of the AFC circuit 9 to add the output to a voltage value of the AFC circuit 9 which determines a scanning step frequency, so that a change in the oscillation frequency of the numerical control oscillator 2 is made faster.

**[0026]** The CNR measuring circuit 10 receives the baseband signals ID and QD, calculates a dispersion value of the signal point arrangement data obtained from the baseband signals ID and QD, compares the dispersion value with a predetermined threshold value, counts the number (DSMS) of occurrences of a dispersion value in excess of the threshold value per a predetermined unit time, and refers to a table shown in Fig. 10 formed through experiments by using the occurrence frequency (DSMS) as a search key to thereby obtain a C/N value which is output as a 2-bit CNR code. For example, as shown in Fig. 11, the CNR code takes a value "00" at a high CNR equal to or larger than 9dB, a value "01" at an intermediate CNR equal to or larger than 4dB and smaller than 9dB, and a value "10" at a low CNR smaller than 4 dB.

**[0027]** The logical gate circuit 11 receives the signals AI and AO output from the frame sync timing circuit 4 and the CNR code output from the CNR measuring circuit 10, and outputs the carrier filter control signal (CRFLGP) and gain control signal (GCONT).

**[0028]** More specifically, as shown in Fig. 12, the logical gate circuit 11 has: NAND gates 111, 112 and 113 for receiving the CNR code and outputting signals corresponding to the high, intermediate and low C/N values; an OR gate 114 for receiving the signals AI and AO and outputting a signal G such as shown in Fig. 2(d) which takes a high potential in the sections of the BPSK signal, burst symbol signal and QPSK signal; an inverter 115 for outputting a high potential signal at the high C/N value; a NAND gate 116 for outputting the signal G at the intermediate C/N value; a NAND gate 117 for outputting the signal AI at the low C/N value; an OR gate 118 for receiving the outputs from the inverter 115 and NAND gates 116 and 117 and outputting the carrier filter control signal (CRFLGP); and a NAND gate 119 for outputting the high potential gain control signal (GCONT) at the high or low CNR.

**[0029]** At the high C/N value, the logical gate circuit

- 11 outputs the high potential carrier filter control signal (CRFLGP) irrespective of the discriminated mode (in any section of the header, burst symbol signal, QPSK signal and 8PSK signal), at the intermediate C/N it outputs the high potential carrier filter control signal (CRFLGP) in any section of the header, burst symbol signal and QPSK signal, and at the low C/N it outputs the high potential carrier filter control signal (CRFLGP) in any section of the header and burst symbol signal. In other cases, the low potential carrier filter control signal (CRFLGP) is output. The logical gate circuit 11 also outputs the high potential gain control signal (GCONT) at the high or intermediate C/N, and the low potential gain control signal at the low C/N.
- 5 **[0030]** When the high potential carrier filter control signal (CRFLGP) is output, the carrier filter 8 executes a filtering operation to smooth and output the phase error voltage. When the low potential carrier filter control signal (CRFLGP) is output, the carrier filter 8 stops the filtering operation so that the output immediately before the stop is held and output. When the high potential gain control signal (GCONT) is output, the gain control circuit 8 amplifies the output of the carrier filter 7 two times and outputs it. When the low potential gain control signal (GCONT) is output, the gain control circuit 8 outputs the output of the carrier filter 7 as it is.
- 10 **[0031]** In the hierarchical transmission digital demodulator of this invention constructed as above, the baseband signals i and q are multiplied by the arithmetic circuit 1 by the orthogonal reproduction carriers output from the numerical control oscillator 2 so that the frequencies of the baseband signals i and q are tuned and the baseband signals are supplied as the baseband signals ID and QD to the frame sync timing circuit 4 via the roll-off filter 3. The frame sync timing circuit 4 supplies the TMCC pattern to the transmission mode judging circuit 5 which decodes the TMCC pattern to supply the transmission mode signal to the frame sync timing circuit 4.
- 15 **[0032]** Upon reception of the baseband signals ID and QD and transmission mode signal, the frame sync timing circuit 4 detects the frame sync pattern and outputs the frame sync signal SYNC and signals AI and AO. The frame sync signal SYNC is supplied to the gain control circuit 8 so that each time the frame sync is detected, the operation of the gain control circuit 8 is reset. The signals AI and AO are supplied to the carrier reproduction phase error detection circuit 6 and logical gate circuit 11.
- 20 **[0033]** Upon reception of the baseband signals ID and QD and signals AI and AO, the carrier reproduction phase error detection circuit 6 selects a proper phase error table in accordance with the baseband signals and signals AI and AO to detect the phase error voltage which is supplied to the carrier filter 7 to be smoothed. Upon reception of the baseband signals ID and QD, the CNR measuring circuit 10 counts the number DSMS in accordance with the signal point arrangement of the
- 25
- 30
- 35
- 40
- 45
- 50
- 55

baseband signals ID and QD. In accordance with the counted DSMS, the C/N value is obtained and output as the CNR code.

**[0034]** Upon reception of the CNR code and signals AI and AO, the logical gate circuit 11 checks whether the C/N value is the high, intermediate or low C/N value. If the CN value is either the high or intermediate C/N value, the gain control signal (GCONT) is supplied to the gain control circuit 8 to set a high loop gain of the gain control circuit 8 so that the phase error voltage output from the carrier filter 7 is amplified two times and output. If the logical gate circuit 11 judges the C/N value as the low C/N value, the gain control signal (GCONT) controls the gain control circuit 8 to take a low loop gain so that the phase error voltage output from the carrier filter 7 is output as it is.

**[0035]** Upon reception of an output from the gain control circuit 8, the cumulative adder 91 of the AFC circuit 9 cumulatively adds the output voltage of the gain control circuit 8 to the voltage value generated by the AFC circuit which voltage value determines the scanning step frequency. Therefore, the oscillation frequency of the numerical control oscillator 2 is changed so that the frequency scanning width is changed and then reproduction carrier frequency is changed.

**[0036]** Next, the operation of the hierarchical transmission digital demodulator of this invention constructed as above will be described with reference to the flow chart of Fig. 13.

**[0037]** As the power is turned on, the AFC circuit 9 scans the frequency to change the reproduction carrier frequency (Step S1), and this frequency scan at Step S1 continues until a frame sync pattern is detected (Step S2). When the frame sync pattern is detected, a burst demodulation mode starts demodulating the BPSK signal and burst symbol signal (Step S3). After Step S3, reception C/N is measured (Step S4).

**[0038]** After the reception C/N value is measured at Step S4, it is checked whether the frame sync signal FSYNC is detected a plurality of times in succession (Step S5). If the frame sync signal FSYNC is not detected a plurality of times in succession, it is judged that the frame sync is not established and the flow returns to Step S1 to repeat the above operations. If the frame sync signal FSYNC is detected a plurality of times in succession, after Step S5 the transmission mode is analyzed in accordance with a decode output of the TMCC pattern (Step S6).

**[0039]** After Step S6 it is checked whether the reception C/N value takes a high C/N value (Step S7). If it is judged at Step S7 that the reception C/N value takes the high C/N value, demodulation for each hierarchy or continuous demodulation is performed (Step S8). Next, the gain of the gain control circuit 8 is set to a high loop gain (Step S9) to thereafter return to Step S4 to repeat the above operations.

**[0040]** At Steps S7 to S9, a high potential signal output from the inverter 115 is output as the carrier filter

control signal (CRFLGP) so that the carrier filter 7 is controlled to be in an operation state to sequentially demodulate the sections of the header, burst symbol signal, QPSK signal and 8PSK signal in this input order. In this case, the NAND gate 119 outputs a high potential signal as the gain control signal (GCONT) so that the gain control circuit is controlled to be in a high gain state.

**[0041]** If it is judged at Step S7 that the reception C/N value is not the high C/N value, it is then judged whether the reception C/N value is an intermediate C/N value or not (Step S10). If it is judged at Step S10 that the reception value is not the intermediate C/N value, the flow reruns to Step S2 to repeat the above operations. If it is judged at Step S10 that the reception value is not the intermediate C/N value, it means the low C/N value so that the NAND gate 119 outputs a low potential signal as the gain control signal (GCONT) to control the gain control circuit 8 to be in a low gain state.

**[0042]** Also, in the state of the low C/N value, a high potential signal is output from the NAND gate 117 as the carrier filter control signal (CRFLGP) to control the carrier filter 7 to be in an operation state. Therefore, in response to an output from the carrier filter 7, the sections of the header and burst symbol signal, i.e., the sections of the BPSK signal (including the burst symbol signal), are demodulated.

**[0043]** If it is judged at Step S10 that the reception C/N value is the intermediate C/N value, it is checked whether the low hierarchical signal is the QPSK signal or not (Step S11). If it is judged at Step S11 that the low hierarchical signal is the QPSK signal, a high potential signal is output from the NAND gate 116 as the carrier filter control signal (CRFLGP) to control the carrier filter 7 to be in an operation state. In response to the output from the carrier filter 7 in the operation state, the sections of the header, burst symbol signal and QPSK signal, i.e., the sections of the G timing shown in Fig. 2(d), are sequentially demodulated (Step S13).

**[0044]** After Step S13, a high potential signal is output from the NAND gate 119 as the gain control signal (GCONT) to control the gain control circuit 8 to be in a high gain state to thereafter return to Step S4 to repeat the above operations (Step S14).

**[0045]** If it is judged at Step S11 that the low hierarchical signal is not the QPSK signal, it means the 8PSK signal. Therefore, The OR gate 118 outputs a low potential signal as the carrier filter control signal (CRFLGP) to stop the operation of the carrier filter, and a high potential signal is output from the NAND gate 119 as the gain control signal (GCONT) to control the gain control circuit 8 to be in a high gain state to thereafter return to Step S4 to repeat the above operations (Step S12).

**[0046]** As described so far, according to the hierarchical transmission digital demodulator of the embodiment of the invention, during the period until sync capture is established, the carrier is reproduced in

accordance with the demodulation output for the sections of the header and burst symbol signal. Therefore, carrier can be reproduced with reliable and good sync capture performance. If after the sync capture, the reception C/N value measured by the CNR measuring circuit 10 is high, the carrier is demodulated in accordance with a continuous demodulation output. Therefore, it is possible to prevent jitters from being generated by frequency variation while the carrier filter is held in suspension during the burst demodulation mode. If after the sync capture, the reception C/N value is intermediate, the carrier is demodulated in accordance with the demodulation output of the hierarchy signals except the 8PSK signal. Therefore, the carrier can be reproduced stably in accordance with the main signal (QPSK).

**[0047]** According to the hierarchical transmission digital demodulator of the embodiment of the invention, different carrier reproduction loop characteristics are used being switched between the carrier reproduction before and after the sync capture. The carrier can therefore be reproduced properly, stably and reliably.

#### INDUSTRIAL APPLICABILITY OF THE INVENTION

**[0048]** As described so far, according to the hierarchical transmission digital demodulator of the invention, during the period until frame sync is captured, a reliable carrier reproduction is possible, and after the frame sync is captured, the carrier is reproduced at a high C/N value in accordance with the continuous demodulation output. It is therefore possible to prevent jitters from being generated. If the C/N value is intermediate after the frame sync is captured, the carrier is reproduced in accordance with the demodulation output for hierarchical signals except the high hierarchical signal. It is therefore possible to reproduce the carrier for the necessary hierarchical signals stably without jitters.

#### **Claims**

1. A hierarchical transmission demodulator comprising: first carrier reproducing means for reproducing a carrier in accordance with demodulation outputs that a modulated wave in for a header section and a modulated wave of a burst symbol signal are demodulated; C/N measuring means for measuring a reception C/N value; second carrier reproducing means for reproducing the carrier in accordance with the demodulation outputs if the measured reception C/N value after sync capture is equal to or larger than a first predetermined threshold; and third carrier reproducing means for reproducing the carrier in accordance with demodulation signals at a hierarchical level except a high hierarchical level if the measured reception C/N value after the sync capture is equal to or larger than a second threshold which is lower than the first threshold.

2. A hierarchical transmission digital demodulator according to claim 1, further comprising reproduction loop characteristic switching means for switching a carrier reproduction characteristic to a different carrier reproduction characteristics during a carrier reproduction by said first carrier reproducing means and during carrier reproduction by the carrier reproducing means different from said first carrier reproducing means.
3. A hierarchical transmission demodulator for demodulating a modulated wave to reproduce a carrier, wherein carrier reproduction after a sync capture is performed in accordance with demodulation outputs corresponding to a measured C/N value after the sync capture which is obtained by C/N measuring means for measuring a reception C/N value.

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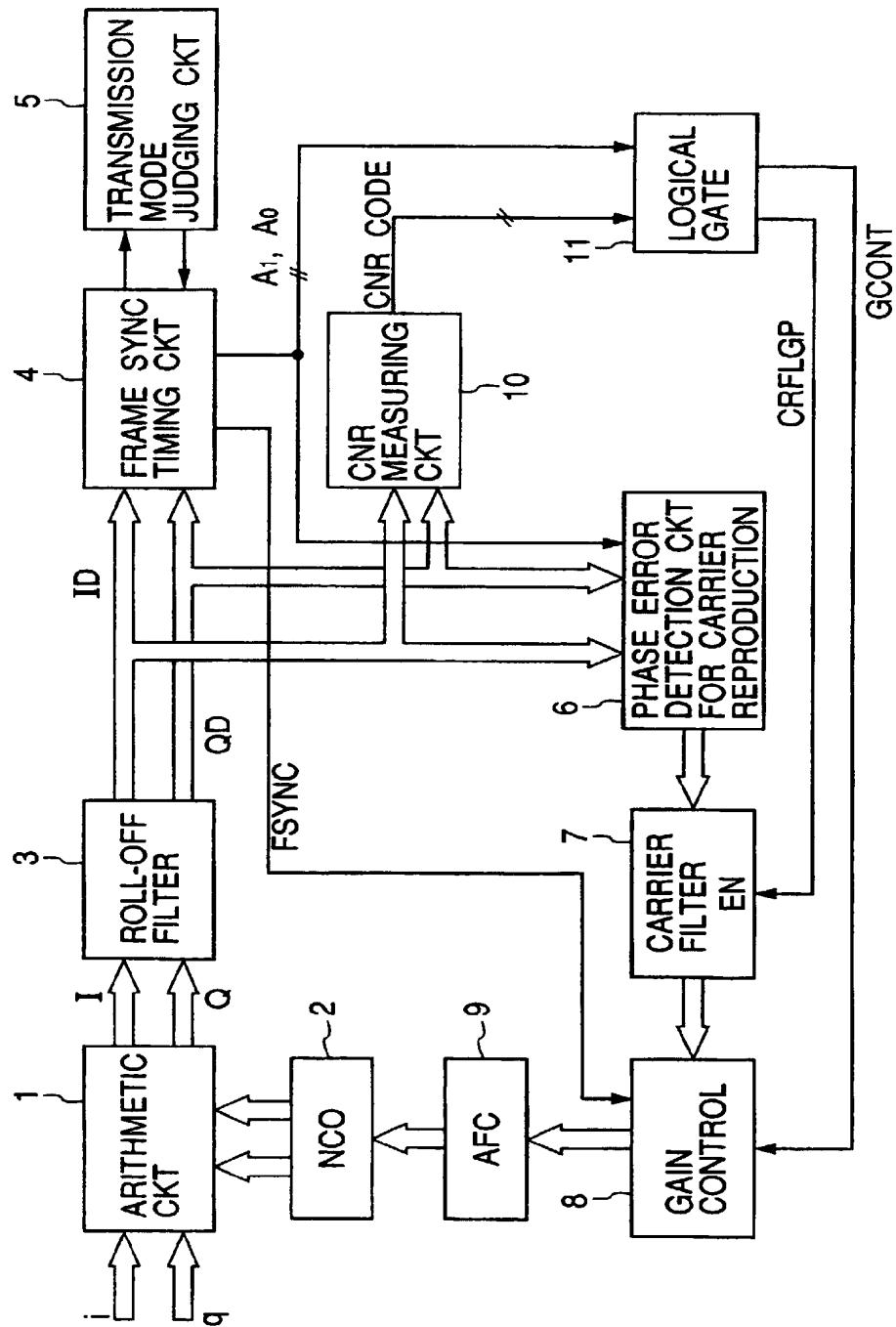
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FIG. 1



*FIG. 2(a)*

SYNC PATTERN (BPSK)	TMCC (BPSK)	SUPERFRAME IDENTIFICATION (BPSK)	MAIN SIGNAL (TC8PSK)	MAIN SIGNAL BS (TC8PSK)	MAIN SIGNAL BS (QPSK)	MAIN SIGNAL BS (QPSK)
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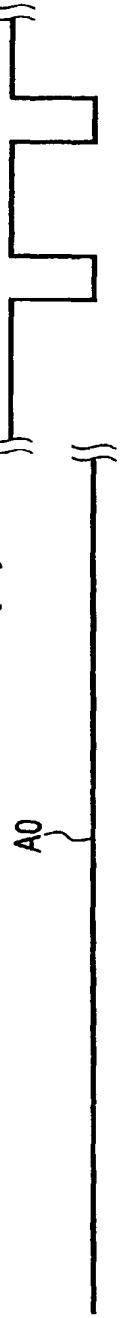
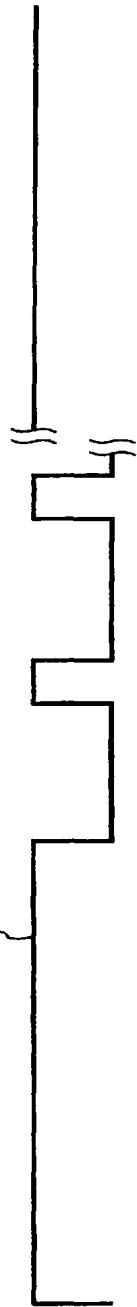
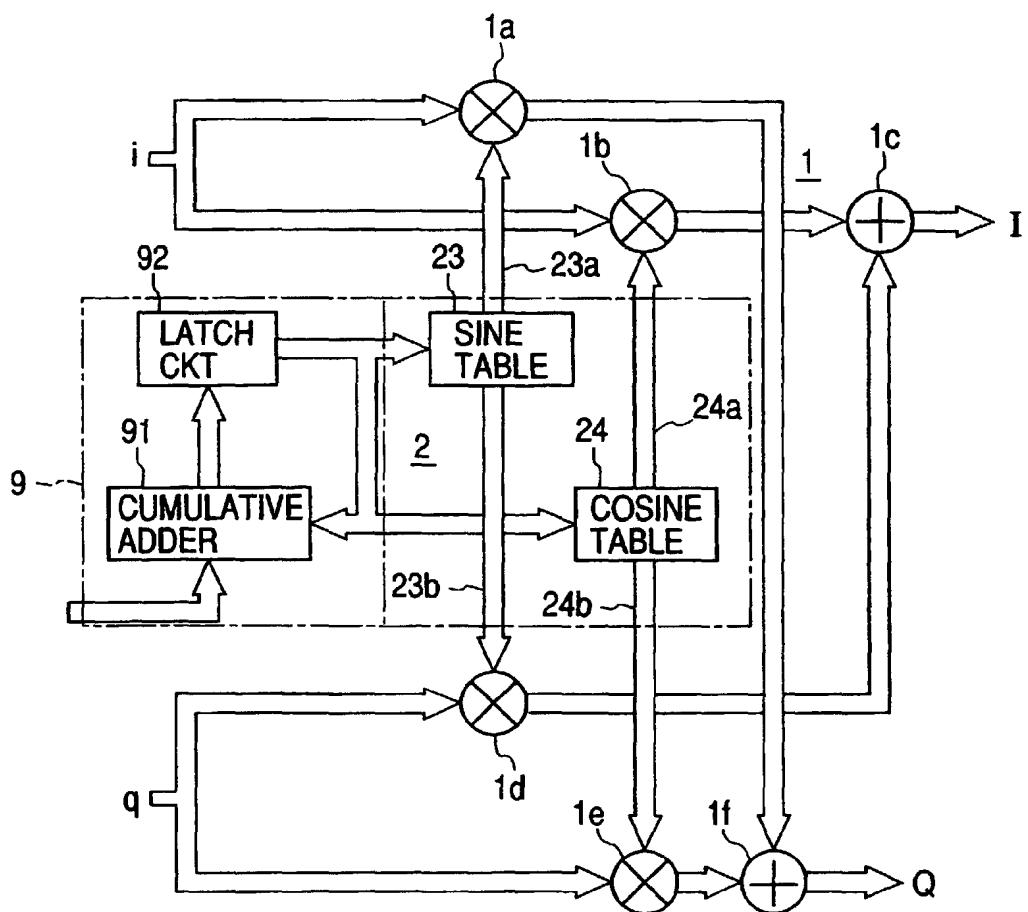
*FIG. 2(b)**FIG. 2(c)**FIG. 2(d)*

FIG. 3



*FIG. 4*

TRANSMISSION MODE	HIERARCHICAL COMBINATION
00	8PSK
01	QPSK
10	8PSK+QPSK
11	8PSK+BPSK

*FIG. 5*

DEMODULATION ROM TABLE	A1	A0
8PSK	0	0
QPSK	0	1
BPSK	1	0

*FIG. 6*

LOOP GAIN	LOGIC
HIGH	H
LOW	L

FIG. 7(a)

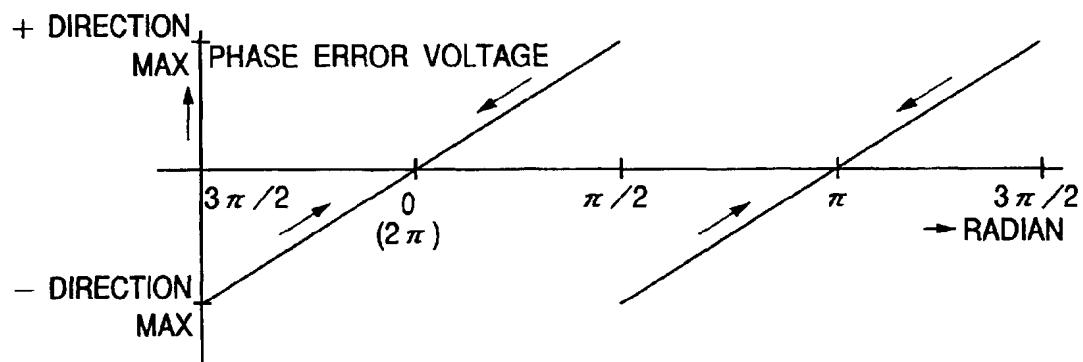


FIG. 7(b)

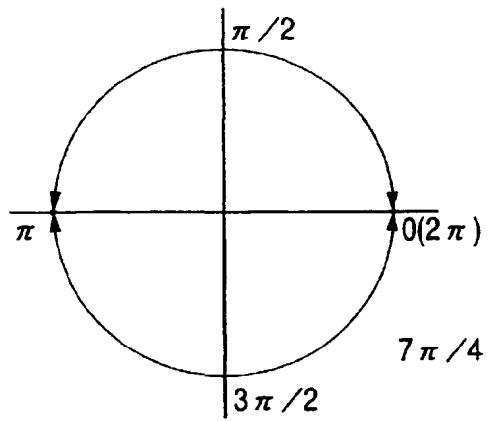


FIG. 8(a)

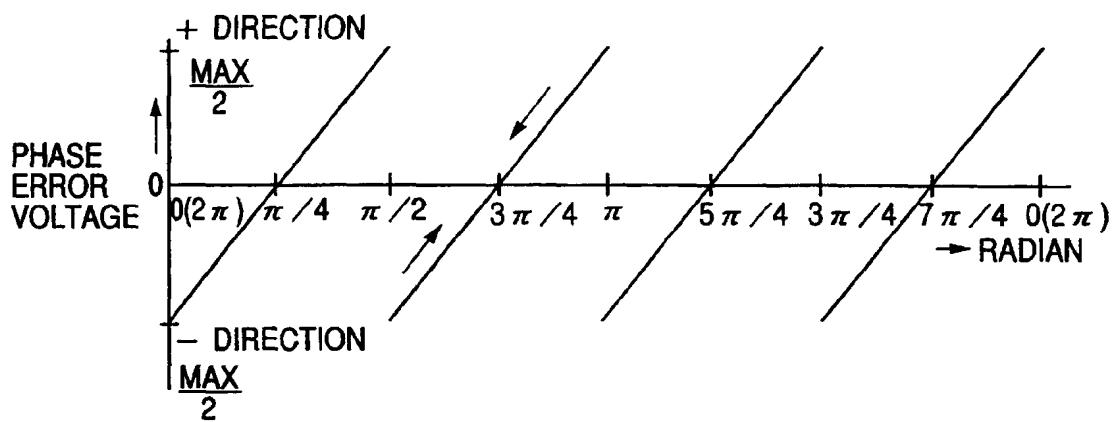


FIG. 8(b)

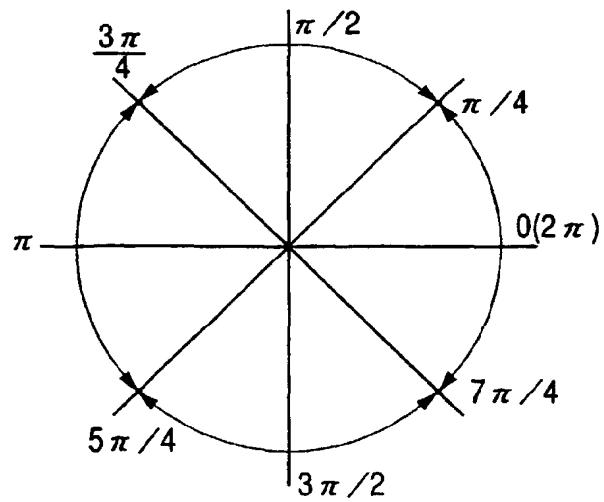


FIG. 9(a)

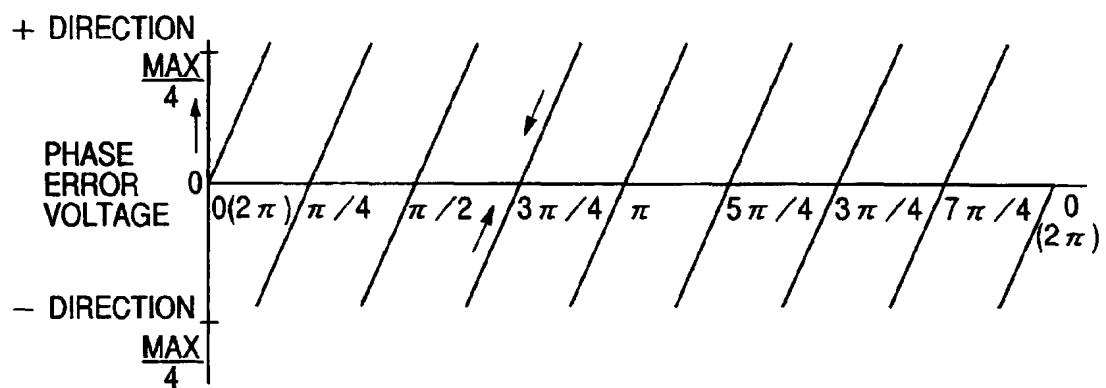


FIG. 9(b)

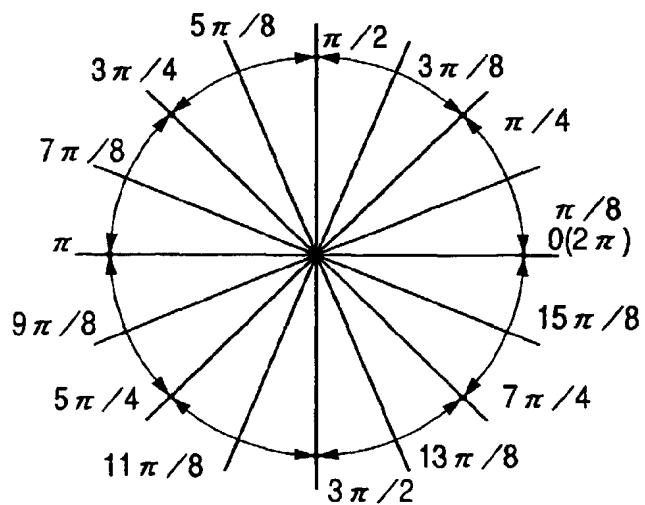
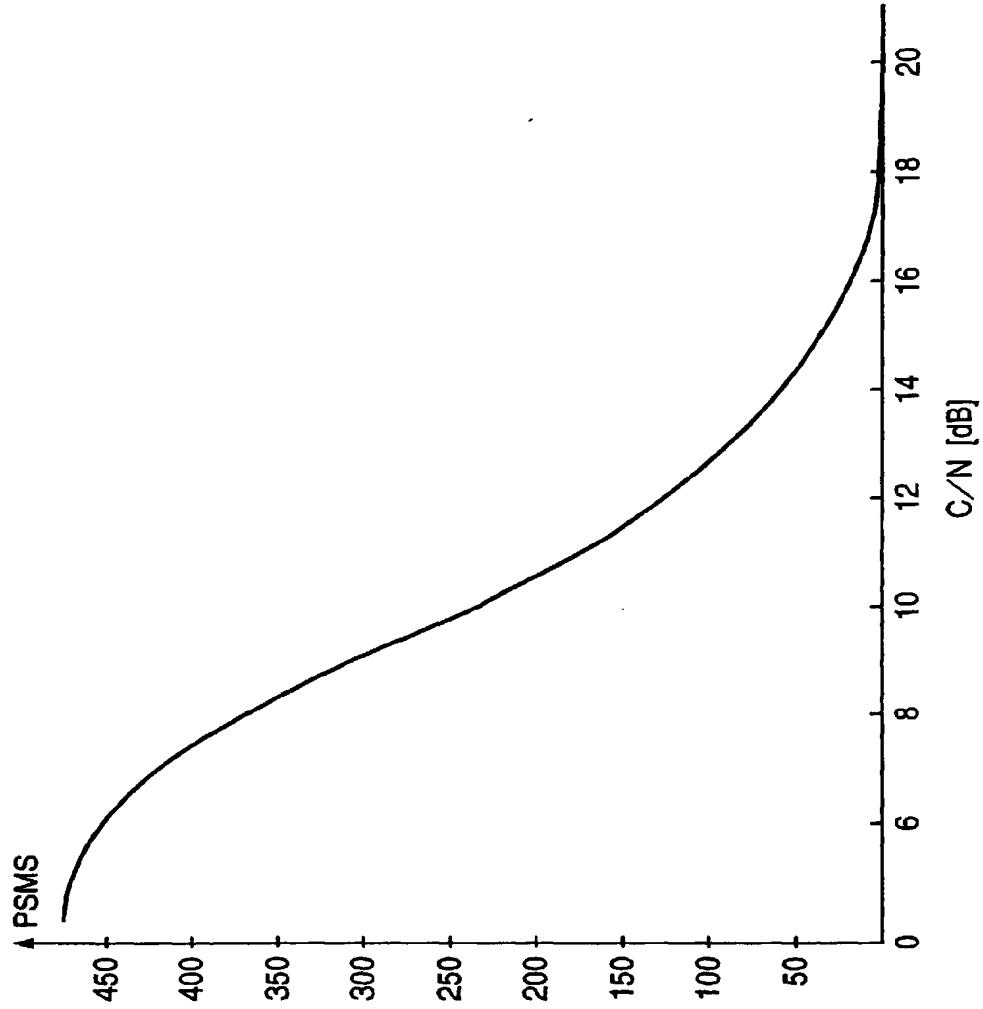


FIG. 10



***FIG. 11***

CNR CODE	CNR RANGE
00	HIGH CNR $\geq$ 9dB
01	9dB>INTERMEDIATE CNR $\geq$ 4dB
10	LOW CNR<4dB

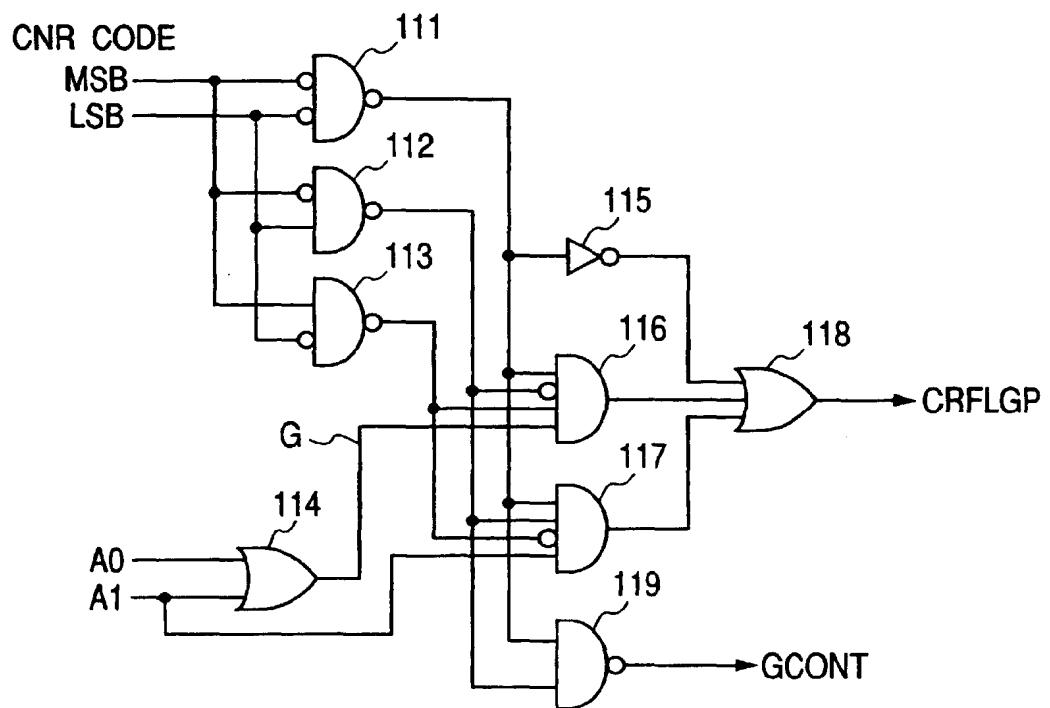
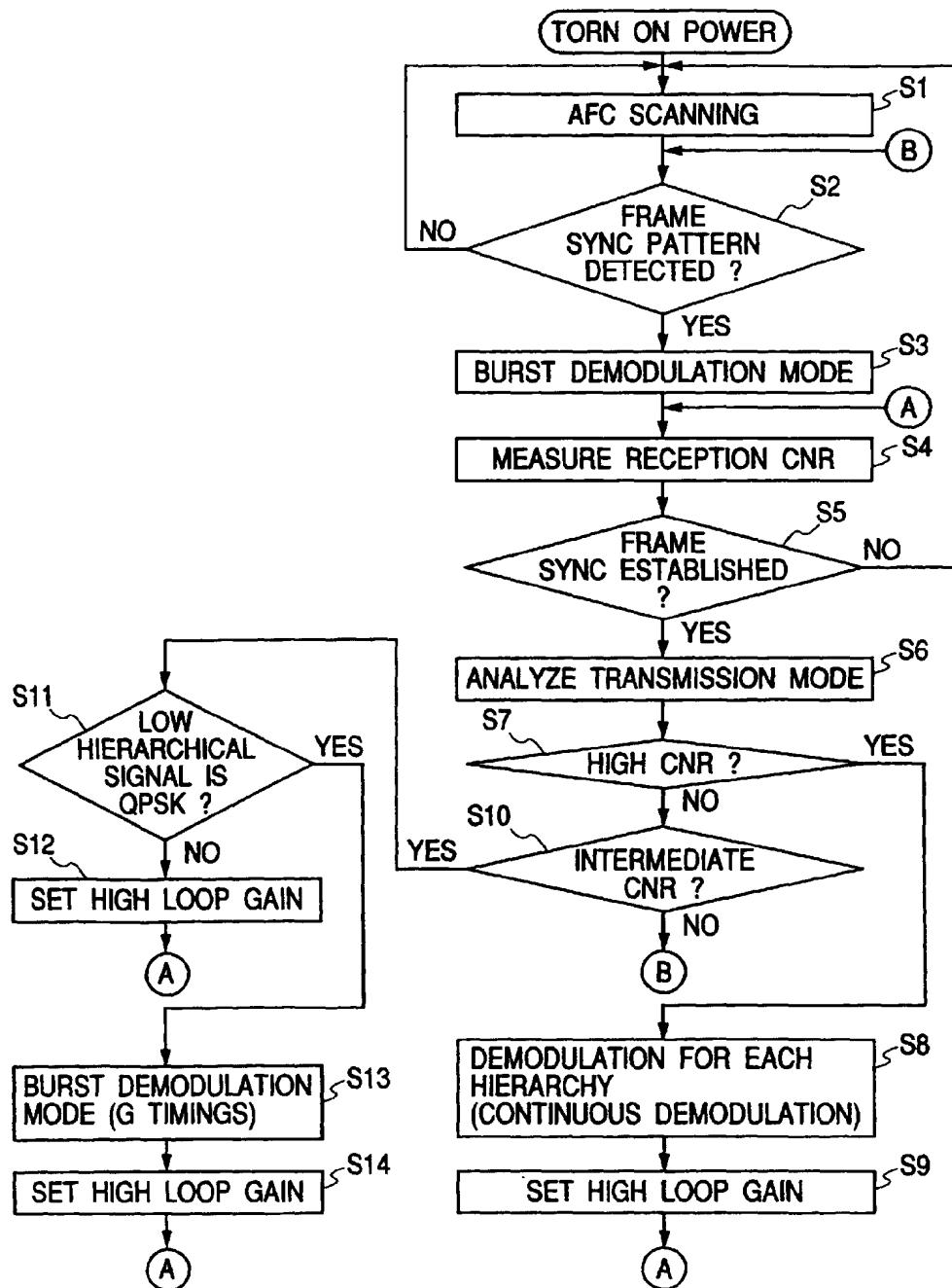
***FIG. 12***

FIG. 13



INTERNATIONAL SEARCH REPORT		International application No. PCT/JP98/05379
<b>A. CLASSIFICATION OF SUBJECT MATTER</b> Int.Cl <sup>6</sup> H04L27/22		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) Int.Cl <sup>6</sup> H04L27/00-27/38		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Jitsuyo Shinan Koho 1926-1998 Kokai Jitsuyo Shinan Koho 1971-1998		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 5-327807, A (Matsushita Electric Industrial Co., Ltd.), 10 December, 1993 (10. 12. 93), Page 10, left column, line 45 to right column line 45 ; Figs. 38, 41 & EP, 506400, B1 & DE, 69223541, E & US, 5600672, A & US, 5555275, A & CN, 1066946, A	3
Y	JP, 55-6965, A (Tokyo Shibaura Electric Co., Ltd.), 18 January, 1980 (18. 01. 80), Page 2, lower right column, line 17 to page 3, upper left column, line 2 ; Fig. 11 (Family: none)	3
A	JP, 9-321813, A (Nippon Hoso Kyokai), 12 December, 1997 (12. 12. 97), Page 4, right column, lines 6 to 18 ; Fig. 1 (Family: none)	1-3
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed		
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 23 February, 1999 (23. 02. 99)		Date of mailing of the international search report 9 March, 1999 (09. 03. 99)
Name and mailing address of the ISA/ Japanese Patent Office		Authorized officer
Facsimile No.		Telephone No.

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## INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/05379

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 63-234759, A (Hitachi, Ltd.), 30 September, 1988 (30. 09. 88), Page 2, lower left column, lines 7 to 13 ; Fig. 1 & US, 4856027, A & CA, 1303691, C	1-3
A	JP, 5-145588, A (Toshiba Corp.), 11 June, 1993 (11. 06. 93), Page 3, left column, lines 32 to 46 ; Fig. 1 (Family: none)	1-3

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